High Performance Matrix Inversion Based on LU Factorization for Multicore Architectures

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ABSTRACT

The goal of this paper is to present an efficient implementation of an explicit matrix inversion of general square matrices on multicore computer architecture. The inversion procedure is split into four steps: 1) computing the LU factorization, 2) inverting the upper triangular U factor, 3) solving a linear system, whose solution yields inverse of the original matrix and 4) applying backward column pivoting on the inverted matrix. Using a tile data layout, which represents the matrix in the system memory with an optimized cache-aware format, the computation of the four steps is decomposed into computational tasks. A directed acyclic graph is generated on the fly which represents the program data flow. Its nodes represent tasks and edges the data dependencies between them. Previous implementations of matrix inversions, available in the state-of-the-art numerical libraries, are suffer from unnecessary synchronization points, which are non-existent in our implementation in order to fully exploit the parallelism of the underlying hardware. Our algorithmic approach allows to remove these bottlenecks and to execute the tasks with loose synchronization. A runtime environment system called QUARK is necessary to dynamically schedule our numerical kernels on the available processing units. The reported results from our LU-based matrix inversion implementation significantly outperform the state-of-the-art numerical libraries such as LAPACK (5X), MKL (5X) and ScaLAPACK (2.5X) on a contemporary AMD platform with four sockets and the total of 48 cores for a matrix of size 24000. A power consumption analysis shows that our high performance implementation is also energy efficient and substantially consumes less power than its competitors.

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1. INTRODUCTION

Forsythe, Malcolm, and Moler [?, p. 31] famously pointed out that "In the vast majority of practical computational problems, it is unnecessary and inadvisable to actually compute A^{-1}". The minority of the cases where the explicit inverse is needed include parameter estimation [?, sec. 7.5], mathematical modeling [?, p. 342ff], computing matrix sign function [?], and polar matrix decomposition [?]. Additional applications of explicit inverse come from wireless networks design [?, ?, ?, ?], optimal control theory [?, ?], and signal analysis [?]. Even though the explicit matrix inversion is not as numerically stable as the application of the L and U factors [?, ?], the loss of a few digits of accuracy is often justified in the above applications. Pair-wise pivoting, on the other hand, introduces a prohibitive loss of accuracy [?] and hence is a poor choice for matrix inversion. We therefore make use of partial pivoting version of tile LU factorization [?] that gives satisfactory accuracy for the L and U factors. From the purely performance-oriented perspective, explicit inverse has a clear advantage. In order to apply the computed inverse on a multi-column matrix of unknowns, one should use a BLAS routine called GEMM [?, ?, ?] that efficiently implements a matrix-matrix multiplication operation. On the other hand, an implicit application of inverse by applying L and U factors from the LU decomposition calls for the TRSM routine from Level 3 BLAS. While both operations may be implemented with affine and properly nested loops, the latter is always at the disadvantage as it has inherent loop-carried data dependencies and achieves a substantially smaller percentage of the peak performance of a given system.

This paper introduces a new implementation of the LU-based matrix inversion. The standard numerical algorithm, as it is implemented in LAPACK [?], is composed of four stages: 1) calculating the LU factorization, 2) inverting the upper triangular U factor, 3) solving a linear system, whose solution yields inverse of the original matrix and 4) applying backward column pivoting on the inverted matrix. Based on block formulation, this standard algorithm is characterized by artifactual synchronization points imposed not only between the different stages but also within each stage, due to the expensive fork-join paradigm. By the same token, the parallelism clearly becomes limited and the algorithm can simply not exploit and fully benefit from the fine-grain parallelism offered by the underlying multicore hardware. To overcome those bottlenecks, tile algorithms have shown promising results by drastically weakening the synchronization points as well as by exposing more parallelism to the user. Applied to the LU-based matrix inversion algorithm, the whole computation is split into fine-grain loosely-coupled computational tasks. The program data flow can then be represented as a directed acyclic graph, where nodes represent tasks and edges the data dependencies between them. A dynamic runtime system QUARK [?] is used to efficiently schedule the various tasks across the available processing units. This may actually result to an out-of-order scheduling, where tasks from multiple stages can concurrently run.

The results reported in this paper are unprecedented. Our high performance implementation achieves a 5-fold improvement against LAPACK with multithreaded MKL BLAS as well as Intel MKL and a 2.5-fold improvement against ScaLAPACK on a quad-socket AMD Opteron Magny-Cours Processor with a total of 48 cores for a matrix of size 24000. A study on power consumption is also provided showing that our high performance algorithm is also energy efficient and substantially consumes less power than the numerical libraries aforementioned.

The reminder of the paper is as follows. Section **??** gives a detailed overview of previous projects in this area. Section **??** recalls the block LU-based matrix inversion algorithm, as implemented in LAPACK [?] and explains its main deficiencies. Section **??** describes our new implementations of the matrix inversion using tile algorithms. Section **??** shows some parallel implementations details using the runtime QUARK. Section **??** presents the performance results. Comparison tests are run on shared-memory architectures against the state-of-the-art, high performance dense linear algebra software libraries, LAPACK [?] (open-source package), Intel MKL 10.2 [?] (commercial package) and ScaLAPACK [?]. Section **??** highlights the power efficiency of our high performance implementation. Finally, Section **??** summarizes the results of this paper and presents the ongoing work.

2. RELATED WORK

Matrix inversion has been an established procedure in statistical community [?, ?] but has mostly concerned symmetric positive definite matrices. As mentioned in Section **??**, there are plenty of applications of the explicit inverse for general square matrices and most of the time the numerical accuracy of obtaining the inverse is is satisfactory for the application at hand regardless of the method chosen to compute [?] – provided the original matrix is not singular nor nearly so. The symmetric positive definite matrices that originate in statistics may use Cholesky factorization as the first step of inversion. The performance of such methods have been studied on multicore computers proving tile algorithms to be beneficial for extracting parallelism [?]. The analysis of available concurrency for explicit inversion was performed by using critical paths of multiple variants of the algorithm [?].

Our work complements these efforts by studying performance and power constraints and opportunities when applied to inversion of general matrices.

3. BLOCK LU-BASED MATRIX INVERSION ALGORITHM

Block algorithms in LAPACK [?] were a software solution to the emergence of cache-based architectures. Such algorithms are characterized by a sequence of two computational phases: panel factorization and an update to the trailing submatrix. The former phase uses transformations that memory-bound while the latter applies the accumulated transformations in a block fashion (hence the name) to the trailing submatrix which, by design, is a much more cache friendly operation and, consequently, is compute-bound in practice. This two-phase sequence has an unwelcome feature of requiring unnecessary synchronization points between the steps. This in turn creates a load imbalance which might be alleviated with the look-ahead technique if the existing block-oriented code is rewritten.

The common practice in LAPACK-derived libraries is for the parallelism to be relegated to the BLAS library. Such implementations are customarily categorized as fork-join or bulk synchronous parallelism (BSP). In the end, the block implementation of LU factorization suffers from the atomicity of the pivot selection has further exacerbated the problem of the lack of parallelism and the synchronization overhead. Last but not least, the LAPACK-based implementations also uses the standard column-major layout as is practiced in Fortran. This becomes less appropriate in the current and next generation of multicore architectures due the resulting false sharing of cache lines and increased overload of the Translation Look-aside Buffer (TLB).

A valid parallelization strategy that turned out quite successful in practice [?] involves making all components of the factorization to run in parallel especially the panel factorization which would severely limit the performance for large matrices if execute serially. The success here is more remarkable as the data partitioning for such parallelization is mostly limited to one dimension: across rows in the panel and across columns for the triangular solve. Only the Schur's complement may use good scalability properties of two-dimensional data and work partitioning because it is based on matrix-matrix multiplication that is internal free from data dependencies.

Algorithm **??** shows in detail the operations and BLAS calls involved the block implementation. The four stages of the algorithm are clearly visible and, in LAPACK, they correspond to multiple functions calls. This produces the second set of synchronization points in addition to the synchronization occurring inside each routine.

We show how these synchronization overheads may be rendered unnecessary in the tile-based implementation. While at the same time, we take advantage of the fact the LU factorization is numerically stable, and, in practice, produces a reasonable growth factor.

4. TILE LU-BASED MATRIX INVERSION ALGORITHM

Synchronization reduction as well as fine-grain computations are not an option in a multicore environment anymore and one has to employ those key concepts to fully take advantage of the hardware specifications. This is exactly the aim of tile algorithms in the context of dense linear algebra. The main idea is to split the original dense matrix into tiles as shown in Figure **??**, in which elements are contiguous in memory, in order to drastically remove the overhead of TLB misses, as seen in block algorithms (see Section **??**). The common coarse grain parallelism is then replaced by a fine-grain computation, alleviating all together the artifactual synchronization

Algorithm 1 Block LU-based matrix inversion. A is an $N \times N$ matrix with a panel size of NB.

```
1:  {Stage 1: Compute $A = L \times U$ (DGETRF)}
2:  for $j = 1$ to N step NB do
3:      DGETF2($A_{j:N,j:j+NB-1}$, $IPIV_j$) {Panel factorization}
4:      DLASWP($A_{:,1:j-1}$, $IPIV_j$) {Swap behind the panel}
5:      DLASWP($A_{:,j+1:N}$, $IPIV_j$) {Swap in front of the panel}
6:      DTRSM($A_{j:j+NB-1,j:j+NB-1}$, $A_{j:j+NB-1,j+NB:N}$) {Compute block row of U}
7:      if $j + NB \leq N$ then
8:          DGEMM($A_{j+NB-1:N,j:j+NB-1}$,
9:                $A_{j:j+NB-1,j+NB-1:N}$, $A_{j+NB-1:N,j+NB-1:N}$)
10:     end if
11: end for
12: {Stage 2: Calculate $U^{-1}$ (DTRTRI)}
13: for $j = 1$ to N step NB do
14:     DTRMM($A_{1:j-1,j:j-1}$, $A_{1:j-1,j:j+NB-1}$)
15:     DTRSM($A_{j:j+NB-1,j:j+NB-1}$, $A_{j:j+NB-1,j+NB:N}$)
16:     DTRTI2($A_{j:j+NB-1,j:j+NB-1}$)
17: end for
18: {Stage 3: Solve the equation $A^{-1} \times L = U^{-1}$ for $A^{-1}$}
19: for $j = N$ to 1 step -NB do
20:     {Copy current block column of L to WORK and replace with zeros}
21:     DLACPY($WORK_{j:N,1:NB}$, $A_{j:N,j:j+NB-1}$
22:     DLASET($A_{j:N,j:j+NB-1}$, 0
23:     {Compute current block column of $A^{-1}$}
24:     if $j + NB \leq N$ then
25:         DGEMM($A_{1:N,j+NB:N}$,
26:               $WORK_{j+NB:N,1:NB}$, $A_{1:N,j:j+NB-1}$)
27:     end if
28:     DTRSM($WORK_{j:j+NB-1,1:NB}$, $A_{1:N,j:j+NB-1}$)
29: end for{Stage 4: Apply column interchanges}
30: DLASWP($A$, $IPIV$)
```

points. The parallelism is rather brought to the fore and does not reside in the BLAS calls.

Algorithm **??** describes the tile version of the four stages LU-based matrix inversion. The first stage i.e., LU factorization, has been replaced by a tile recursive parallel panel LU factorization, introduced by the authors in [?]. The major differences with the block LU factorization are twofold. The panel computation has been enhanced in terms of level 3 BLAS operations using a parallel recursive scheme. The update of the trailing submatrix now operates on tiles, which increases the degree of parallelism and allows look-ahead techniques. The second stage computes the inverse of the U factor. The LAPACK function call DTRTRI has been *unrolled* to fit the new tile algorithmic design, which generates a multitude of independent tasks and removes, within the stage, the synchronization points aforementioned. And these significant algorithmic changes apply to the third and fourth stage following the same principle.

This new tile implementation of the LU-based matrix inversion considerably weakens the synchronization points *within* each of the four stages. But it can clearly be seen also that the in-between synchronization points may be removed, whenever data dependencies permit. Indeed, the second and third stages can start executing while the first stage has not finished yet. However, the fourth stage i.e., column interchange application, requires that previous stages are totally completed before proceeding, since no practical assump-

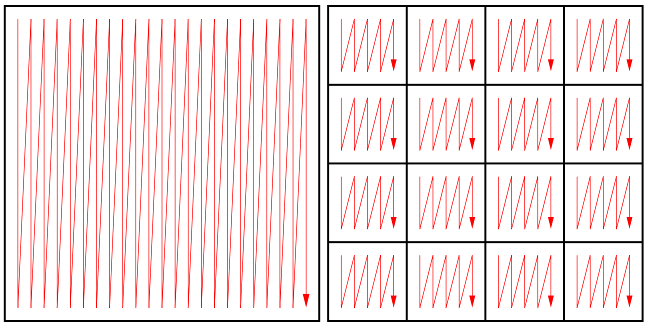


Figure 1: Column-major (left) and tile data layout (right) for a matrix.

tion is possible due to the natural atomicity of the column pivoting operation.

Once the various numerical kernels defined, a runtime environment system becomes crucial to schedule the operations on the available processing units, which is the topic of the next Section.

5. PARALLEL IMPLEMENTATION DETAILS USING THE QUARK FRAMEWORK

Our approach to extracting parallelism is based on the principle of separation of concerns. We define high performance computational kernels and submit them to the QUARK [?] scheduler for parallel execution as dependent tasks.

In fact, the execution flow in our implementation is not driven by a set of loops or recursive calls, as seen in Algorithm **??**, but rather by the data dependencies that are communicated to the QUARK [?] runtime scheduling system in a form of tasks. In practice, this results in an asynchronous out-of-order scheduling. The dynamic runtime environment ensures that enough parallelism is available throughout the entire execution as is assured by the right looking formulation of the algorithm. The advancement of the critical path for the look-ahead purposes, prominently featured in the left looking formulation, is achieved with locality-based task selection and may be enhanced with scheduler hints.

Indeed, computational tasks residing in the critical path (e.g., panel factorization) have a higher priority. On the opposite, the row interchange operations behind the panel during the first stage are not critical to pursue the computation forward and can be delayed as much as possible in favor of critical tasks scheduling. The strict right-looking variant available in LAPACK [?] and ScaLAPACK [?] cannot then be guaranteed anymore. The asynchronous nature of the DAG execution provides sufficient look-ahead opportunities for many algorithmic variants to coexist with each other regardless of the visitation order of the DAG [?].

6. PERFORMANCE RESULTS

This Section reports the performance results on a cutting-edge shared-memory multicore system based on Non Uniform Memory Access (NUMA). Directed acyclic graphs have been also generated along with execution traces to highlight the strength of our high performance implementation. A power consumption study is also presented to show its power efficiency.

6.1 Experimental Setup

Algorithm 2 Tile sequential in-place LU-based matrix inversion. A is an $NT \times NT$ tile matrix.

```
 1: {Stage 1: Compute $A = L \times U$ using parallel recursive panel}
 2: for $k = 0$ to NT−1 do
 3:    CORE_DGETRFR($A_{k,k}$, $IPIV_k$)
 4:    for $n$ = k+1 to NT−1 do
 5:       CORE_DLASWP($A_{k,n}$, $IPIV_k$) {Apply row interchange after the panel}
 6:       for $m$ = k+1 to NT−1 do
 7:          CORE_DGEMM($A_{m,k}$, $A_{k,n}$, $A_{m,n}$)
 8:       end for
 9:    end for
10:    for $n = 0$ to $k-1$ do
11:       CORE_DLASWP($A_{k,n}$, $IPIV_k$) {Apply row interchange behind the panel}
12:    end for
13: end for
14: {Stage 2: Calculate $U^{-1}$ (DTRTRI)}
15: for $m = 0$ to NT−1 do
16:    for $n$ = m+1 to NT−1 do
17:       CORE_DTRSM($A_{m,m}$, $A_{m,n}$)
18:    end for
19:    for $n = 0$ to $m-1$ do
20:       for $k = m+1$ to NT−1 do
21:          CORE_DGEMM($A_{n,m}$, $A_{m,k}$, $A_{n,k}$)
22:       end for
23:       CORE_DTRSM($A_{m,m}$, $A_{n,m}$)
24:    end for
25:    CORE_DTRTRI($A_{m,m}$)
26: end for
27: {Stage 3: Solve the equation $A^{-1} \times L = U^{-1}$ for $A^{-1}$}
28: for $k$ = NT−1 to 0 step −1 do
29:    for $m$ = k to NT−1 do
30:       CORE_DLACPY($WORK_m$, $A_{m,k}$)
31:       CORE_DLASET($A_{m,k}$, 0)
32:    end for
33:    for $m = 0$ to NT−1 do
34:       for $p$ = k+1 to NT−1 do
35:          CORE_DGEMM($A_{m,p}$, $W_p$, $A_{m,k}$)
36:       end for
37:       CORE_DTRSM($WORK_k$, $A_{m,k}$)
38:    end for
39: end for
40: {Stage 4: Apply column interchanges}
41: for $k$ = NT−1 to 0 step −1 do
42:    for $m = 0$ to NT−1 do
43:       CORE_DLASWP($A_{m,k}$, $IPIV_k$)
44:    end for
45: end for
```

All of our performance experiments were done on a single hardware system that we will call *MagnyCour-48*. *MagnyCour-48* is composed of a mother board with four sockets each featuring an AMD Opteron 6172 processor, code named Magny-Cours. Each processor consisted of twelve cores, which made it 48 cores in total. The operating frequency was 2.1 GHz and the main memory size was 128 GB. The theoretical peak for this machine in double precision arithmetic is 403.2 Gflop/s (8.4 Gflop/s per core). All the results were obtained with the Intel MKL 10.3.2 library which was selected as the best BLAS implementation for this system in terms of sequential and parallel performance.

6.2 Performance Comparisons

We compare five different versions of the *LU* inversion algorithm. First, we present the performances of the two versions that can be used in a shared memory system: the Netlib LAPACK library linked with the multi-threaded BLAS from MKL, as well as the multi-threaded MKL LAPACK version of the algorithm. The results from Figure **??** show that even if the MKL library has a better implementation of the LU factorization, no efforts have been made for the triangular inversion to outperform the Netlib version of LAPACK, resulting in similar performances for both libraries.

Second, we present results obtained with the MKL implementation of SCALAPACK using one process per core and the sequential MKL BLAS internally. This version shows how the distributed memory implementation, with good memory locality by default, performs on a NUMA architecture opposed to a shared-memory implementation. We observe that the performances are far better than the MKL multi-threaded version, but require the user to move to a distributed memory implementation of the algorithm. Finally, we present the results of our algorithms implemented in PLASMA library. For both algorithms, threads are bind linearly to each core thanks to the Hardware Locality library [**?**], HWLOC. This, with the QUARK scheduler, ensures a good data locality and reuse which are necessary to achieve performances on NUMA architectures. It is noteworthy to mention that we could not reproduce the same setup for MKL-based implementations since we do not have access to the software package internals. Furthermore, the *ColMajor* version takes as input the matrix in column major layout as the standard of LAPACK. The LU factorization is then performed on the matrix and a layout conversion to tiles is required to perform the three last stages as well as to return the result to the user in column major layout. The *Tile* version takes directly as input the matrix stored in the block layout format and perform all four stages without changes in the data storage. We observe on the Figure **??** than this layout provides 50Gflop/s more than the *ColMajor* version, and both outperform SCALAPACK for matrix sizes over 5000 to reach more than 60% of efficiency. The block size chosen for these experiments is 280, and 320 for the *Tile* version when the size is over 20000.

6.3 Data Flow Representation using Directed Acyclic Graphs

This section presents the DAGs of the four stages of the `GETRFR + GETRI` operations obtained with the scheduler QUARK. Figure **??** shows the DAGs of the four different stages in the routine: the LU Factorization (Figure **??**), the computation of the inverse of L (Figure **??**), the triangular solve for U^{-1} (Figure **??**) and the column swapping (Figure **??**). Figure **??** shows the interleaving of these four DAGs, with the same color code than the previous ones, when you performed them in an asynchronous way while the scheduler

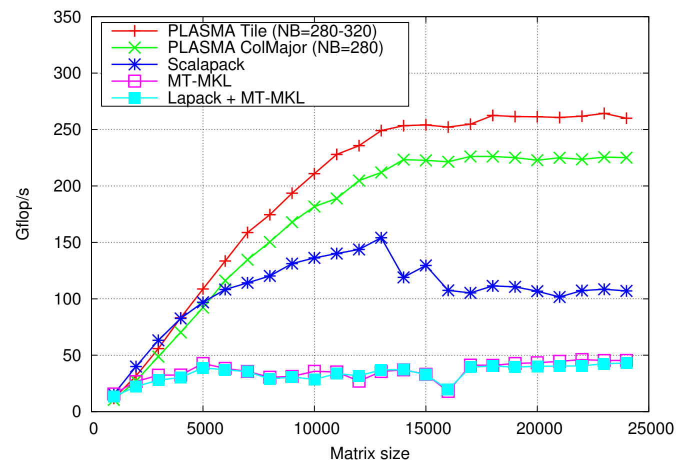


Figure 2: LU-based Matrix Inversion (DGETRF+DGETRI) on *MagnyCour-48*

preserves the dependencies. The nature of the third stage with its backward panel by panel computations naturally delays the beginning of the last stage. Indeed, the first set of swapping are applied, which are to the last column of A, is blocked by the input dependencies of this same block column within the update of the first columns of the stage three (solve for U^{-1}). Then, by limitation of the algorithm to one block column of workspace, the column swapping stage can not proceed before the last step of stage three has started and tiles $A_{m,NT-1}$ with $m \in [0, NT-1]$ have been used for the update.

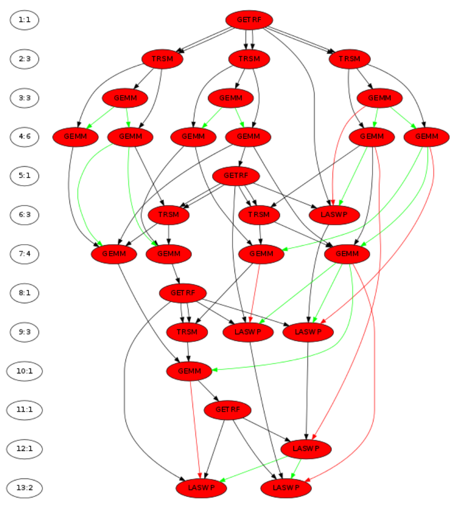
6.4 Execution Traces

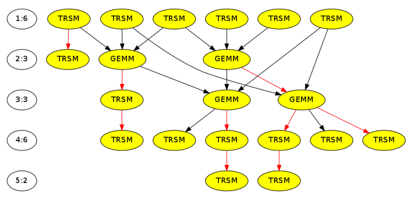
Figure **??** shows the execution traces of the PLASMA LU inversion algorithm with or without synchronization between each stage. For both figures, the LU factorization is in red, the computation of L^{-1} in yellow, the triangular solve for U^{-1} in blue and the column swapping in green. By comparison to the synchronous case shown in Figure **??**, the second trace shown in Figure **??** indicates that the interleaving steps in mainly between the first and the second stages which are respectively the LU factorization and the computation of the inverse of L. This result is expected as shown in the complete DAG of the LU inversion in Figure **??**.

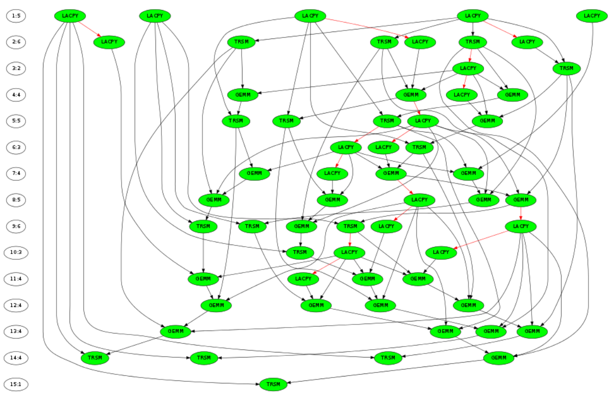
7. POWER PROFILING

The goal of this Section is to show that our high performance implementation is also energy efficient. The experiments have been conducted on a single node of a distributed system named *systemg.cs.vt.edu* from Virginia Tech composed of 324 nodes with Infiniband interconnect. Each node is a dual-socket quad-core Intel Xeon 2.8GHz (2592 cores total) with 8GB of memory. It is actually the largest power-aware compute system in the world. It has over 30 power and thermal sensors per node and relies on PowerPack [**?**] to obtain measurements of the major system components' power consumption (e.g., the CPU, memory, hard disk, and motherboard) using power meters attached to the hardware of the system.

Figures **??**, **??** and **??** show the power consumptions of the LU-based matrix inversion using LAPACK (with multithreaded MKL BLAS), MKL, and PLASMA, respectively. The findings presented below coincide with the analysis of power consumptions in dense linear algorithms studied before [**?**]. In particular, we are able to ob-


(a) DAG for the first stage: LU factorization.


(b) DAG for the second stage: inverse computation of L.


(c) DAG for the third stage: triangular solve for U^{-1}.

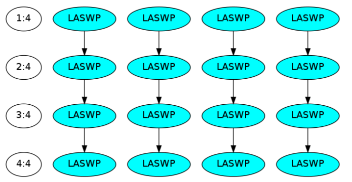

(d) DAG for the fourth stage: column swapping.

Figure 3: DAGs of the four stages composing the `GETRI` operation on a 4-by-4 tiles matrix.

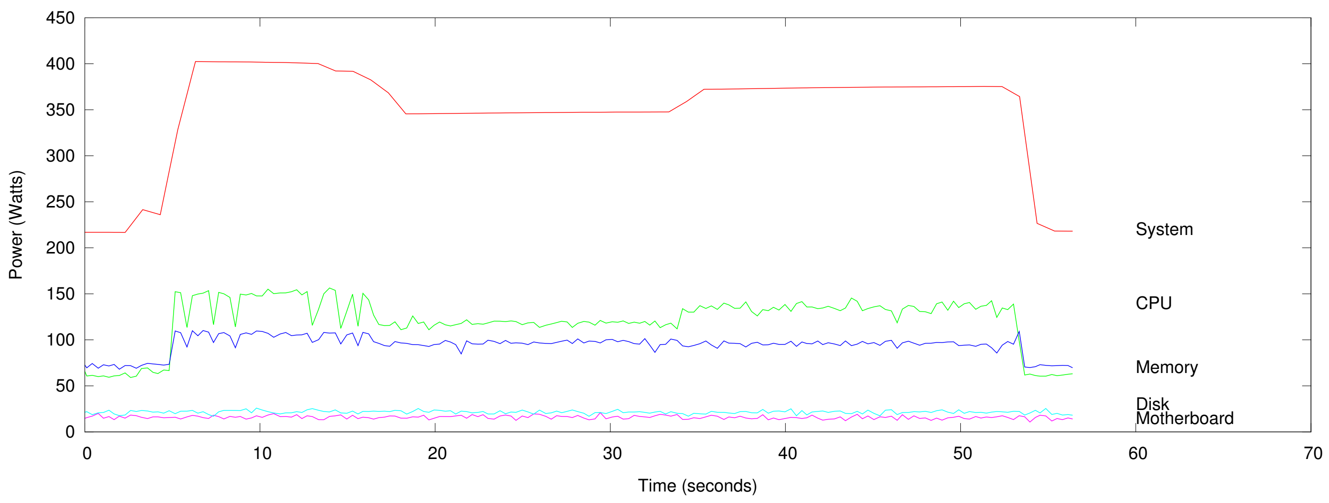


Figure 6: LAPACK LU-based matrix inversion (N=10000) on a dual-socket quad-core Intel Xeon at 2.80GHz (8 cores total).

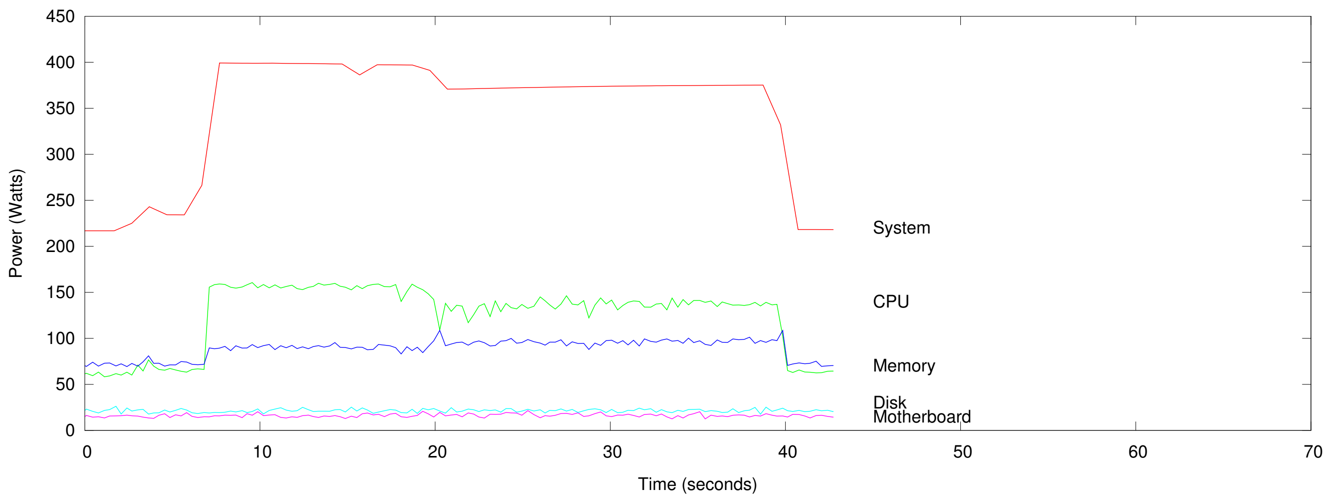


Figure 7: MKL LU-based matrix inversion (N=10000) on a dual-socket quad-core Intel Xeon at 2.80GHz (8 cores total).

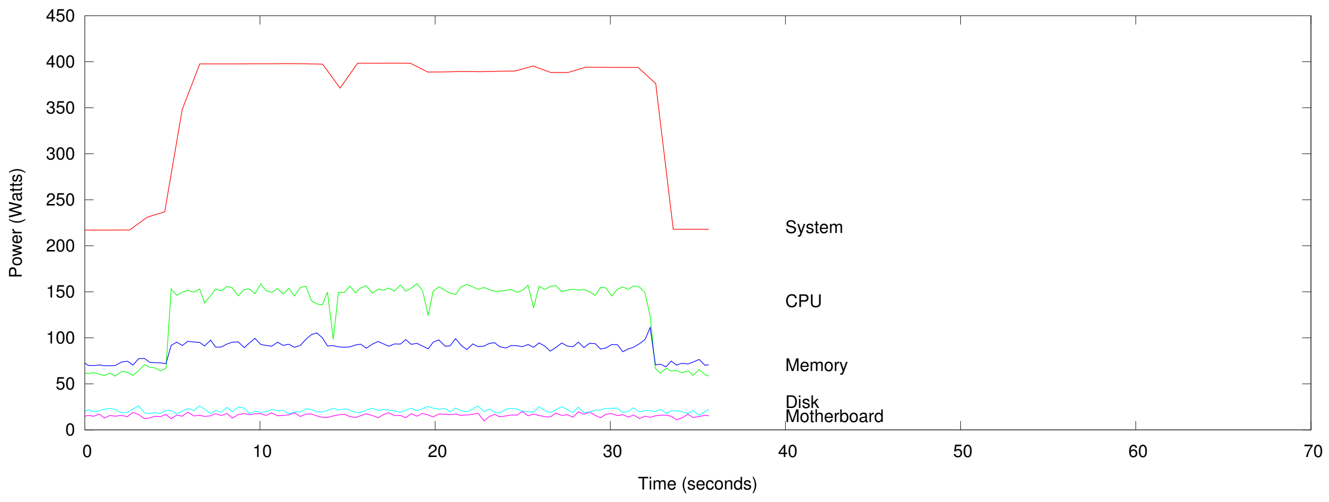


Figure 8: PLASMA LU-based matrix inversion (N=10000) on a dual-socket quad-core Intel Xeon at 2.80GHz (8 cores total).

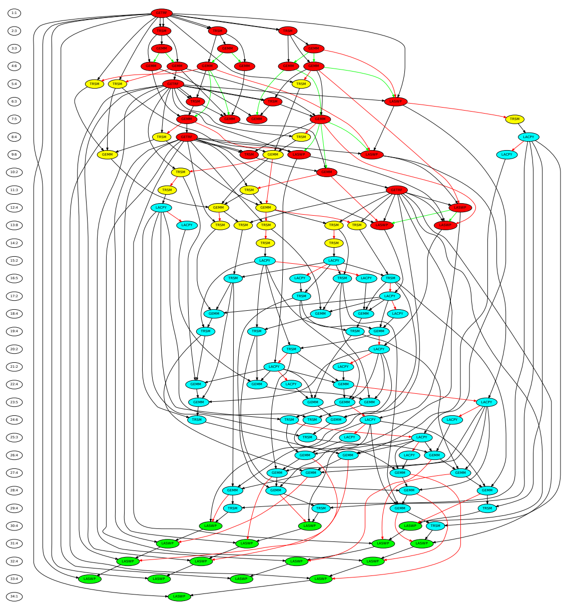
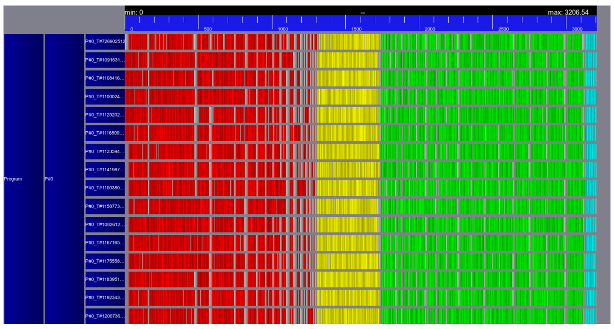
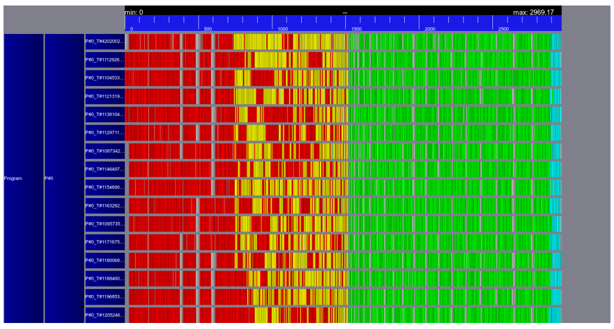


Figure 4: DAG containing the four stages which are interleaved with the dependencies preserved on a 4-by-4 tiles matrix. The same color code as in Figure ?? is used.



(a) With synchronization between each stage.



(b) With interleaved stages.

Figure 5: Execution traces of the `DGETRI` **routine with a 5000-by-5000 matrix and** $NB = 250$ **on a 16-cores architecture.**

serve phases of the computation from the power charts. Although the number of cores is small (i.e., 8 cores total), PLASMA is substantially more power efficient than LAPACK and to a lesser extent than MKL. PLASMA would even consume less power in the context of many cores against it competitors because this is where PLASMA excel the most thanks to the tremendous amount of independent computational tasks generated through tile algorithms.

8. SUMMARY AND FUTURE WORK

We have presented a tile implementation of the matrix inversion algorithm based on LU factorization. Our core shares the desirable numerical properties with the formulations that use partial pivoting. At the same time, however, we introduce plentiful opportunities for parallel execution and data partitioning that is cache-friendly and works well across complex memory hierarchies of multicore architectures. In the end, our approach yields vast improvements from the performance perspective. In fact, we observed many-fold speedup against the best implementations of numerically comparable codes.

As a future direction, we consider extending our methodology to distributed memory machines using a different version of DAG scheduler called DAGuE [**?**, **?**, **?**, **?**, **?**].

9. ACKNOWLEDGMENT

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